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13. ABSTRACT (Maximum 200 words)

The research project has achieved six significant results: (1) fabrication of 10 nm Si pillars array and the first observation of photoluminescence from the Si pillar array fabricated by nanolithography; (2) a new MSM photodetector structure that can achieve 140 GHz in Si -- the fastest photodetectors in crystal Si. (3) proposal and demonstration of a new planar field-induced quantum dot transistor, and observation of interplay of quantum effects and Coulomb effects; (4) the first observation of bias-induced resonant tunneling peak splitting in a quantum dot; (5) demonstration of a new quantum wave bandstop filters, and (6) demonstration of silicon single electron and single Hole Quantum-dot transistors that have operation temperature above 100K.

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I. Objective

The research project has been focusing on investigation and development of (a) new nanofabrication technologies, (b) quantum effects and Coulomb blockage effects in nanodevices, and (c) ultra-fast photodetectors.

II. Summary of Major Accomplishments

The research project, which covers the period from May 1, 1992 to Oct. 1, 1995, has achieved six significant results: (1) fabrication of 10 nm Si pillars array and the first observation of photoluminescence from the Si pillar array fabricated by nanolithography; (2) a new MSM photodetector structure that can achieve 140 GHz in Si -- the fastest photodetectors in crystal Si. (3) proposal and demonstration of a new planar field-induced quantum dot transistor, and observation of interplay of quantum effects and Coulomb effects; (4) the first observation of bias-induced resonant tunneling peak splitting in a quantum dot; (5) demonstration of a new quantum wave bandstop filters, and (6) demonstration of silicon single electron and single Hole Quantum-dot transistors that have operation temperature above 100K. We will briefly describe these results in the following. For more details, please see enclosed reprints and references.

2.1. Fabrication of 10 nm Si Pillars Using e-beam and RIE and PL Investigations

We fabricated free-standing Si pillars with diameters of ~10 nm and aspect ratios greater than 15 and investigated their photoluminescence [3,8]. The pillars were fabricated using electron beam lithography, chlorine based reactive ion etching, and subsequent HF wet etching. Using HF etching offers several advantages: (a) it is relatively independent of stress and therefore preserves the original shape of the structure; (b) it is a room temperature process; (c) it has a very controllable etch rate, ~1.9 nm/hr; and (d) it can remove RIE damage and passivate the Si surface. Photoluminescence with a peak at 720 nm was repeatedly observed from an array of nanoscale pillars with ~ 20 nm diameters. This is the first report on observation of photoluminescence from lithographically fabricated Si nanopillars, yet the cause of such PL is still unclear.

2.2 140 GHz MSM Photodetectors in Si

Previously, we have reported metal-semiconductor-metal photodetectors (MSMPD's) in low-temperature-grown GaAs with a response time of 0.87 ps and a 3-dB bandwidth of 510 GHz, as well as MSMPD's in bulk Si with 3.7 ps and 110 GHz. However, the response of Si MSMPD's is wavelength dependent and the fast response was achieved only at short wavelengths (~ 400 nm). At long wavelengths, such as that of GaAs lasers (~ 800 nm), their bandwidth dropped to ~ 40 GHz. This is because that it will take a long time to collect the photo-generated carriers that are deep inside the semiconductor. This wavelength dependence in response and the slow speed at

long wavelengths impose serious limitations to Si detectors' application. To solve this problem, we fabricated high-speed MSMPD's in thin silicon-on-insulator (SOI) substrates. The thickness of the thin Si is much less than the light penetration depth in Si; the buried oxide acts as a barrier to cut off carriers generated deep inside of the semiconductor substrate. Therefore, the detector speed becomes not only faster, but also independent of light wavelength. Our measurements showed that the detectors with 100 nm finger spacing and 100 nm top Si thickness have a response time of 3.2 ps and a bandwidth of 140 GHz, and the detector's speed is independent of the laser wavelength [4, 10]. This is, to our knowledge, the fastest photodetector on crystalline Si material.

2.3. New Planar Field-induced Quantum-dot Transistor and Observation of Interplay of Quantum Effects and Coulomb effects

We proposed and demonstrated a new field-induced quantum dot transistor that has a nanoscale dot-gate inside the gap of a split-gate [7]. Because of the novel structure and small dot size, strong oscillations in the drain current as a function of the gate bias were observed at temperature up to 4.2 K or with a drain bias up to 5 mV. Temperature dependent study showed that the energy gaps in the dot are as large as 4.5 meV. Simulation indicates that, in the device, quantum size effect and Coulomb effect are comparable; both contribute significantly to the energy gaps in the quantum dot. The new quantum-dot transistor has a nanoscale dot-gate placed inside the gap of a split-gate on top of a heterostructure). The dot-gate, which consists of a dot at the middle of a wire, is positively biased to induce a quantum dot and two one-dimensional wires at the heterostructure interface. The wires connect the dot to the two-dimensional electron gas at the source and the drain. The split-gate is negatively biased to change the number of electrons inside the dot and to make the confinement potential stronger. For a given positive dot-gate bias, the electric field beneath the dot is larger than that beneath the wires, therefore the conduction band edge under the dot is lower than that under the wires, creating a quantum dot attached to two wires.

2.4. Observation of Bias-Induced Resonant Tunneling Peak Splitting in a Quantum Dot

We have observed for the first time that, in a lateral confined quantum dot, as the gate-voltage is scanned, a dc bias across the quantum dot splits each resonant differential conductance peak into two [9]. The separation between the two splitting peaks was found to be nearly a linear function of the applied bias, V_D . The temperature dependent study indicated that the corresponding energy separation between the two splitting peaks is almost equal to eV_D. This splitting can be explained by the bias induced shift of energy levels in the quantum dot and the splitting of the Fermi level. An analytical formula which describes the splitting has been derived and is in a good agreement with experiments. The formula can provides unique information about the energy states in the

quantum dot. Our current work presents significant progress in understanding single electron transistors.

2.5 Quantum Wave Bandstop Filters

We have proposed and demonstrated, based on the concept of a microwave bandstop filter, two quantum wave bandstop filter structures [11]. Both structures employ nanoscale gates in a heterojunction transistor to induce a quantum cavity connected by two one-dimensional wires. As the electron wavelength is changed by the gate-voltage, we observed that, at certain gate-voltages, the transmission of electron waves through the cavity is partially blocked and the drain current drops as large as 50% . This phenomenon is explained in terms of the destructive quantum interference between different electron wave modes in the cavity.

Because of the similarity between electron waves in a quantum waveguide and electromagnetic waves in a microwave waveguide, many microwave device concepts can be instructive in engineering new high functionality quantum devices. Previously, several structures based on such analogy have been proposed and discussed. Examples are a stub-tuning device, a double-bend quantum waveguide, and a cavity coupled to two quantum waveguides. However, most of these studies were limited to the computer simulations and theoretical analysis.
Experimentally, only in stub-tuning devices, weak conductance modulations as a function of gate voltage were observed and attributed to the quantum interference effect. Our current work is the first clear experiment in demonstrate a quantum-wave guide band-stop filter.

2.6 Silicon Single Electron and Single Hole Quantum-dot Transistors With Operation Temperature Above 100K

We have proposed and demonstrated silicon single electron and single hole quantum dot transistors (QDTs) that can operate at a temperature above 110 K [13-15]. The QDT consists of a silicon dot separated from the source and the drain by two constrictions. The silicon dot has a size 8 nm x 30 nm x 30 nm, is surrounded by thermal oxide, and has a gate on top that can change the charge concentration inside the dot. Since the quantum dot has small size, discrete energy levels will be formed. The constriction with a size smaller than that of the quantum dot create the tunneling barriers: one is between the quantum dot and the source and the other is between the quantum dot and the drain. The source and the drain were doped n-type for electron QDTs and p-type for hole QDTs. For electron QDTs, the gate and drain voltage are positive to induce electron in the quantum dot and to drive the electron from the source to the drain. For hole QDTs, the two biases are reversed.

The single-electron quantum dot transistors show oscillation of the drain current as a function of the gate voltage at temperatures up to 170 K and drain biases up to 80 mV. The

oscillation is due to electron tunneling through the discrete energy levels inside the quantum dot. The average energy level spacing is ~ 70 meV. Data analysis shows that the discrete energy level are caused by Coulomb interactive as well as quantum size effects. The single hole quantum dot transistors show similar oscillation up to 110 K and drain biases up to 50 mV. The average energy level spacing is ~ 42 meV.

III. List of Publications

Journal Papers

[1] Y. Wang, and S. Y. Chou, "Engineering Sub-50 nm quantum Effect Devices and Single-electron Transistors Using E-Beam Lithography," *J. Vac. Sci. and Tech.*, **B10**(6), pp 2962-2965, 1992.

[2] P. B. Fischer and S. Y. Chou, "Sub-50 nm High Aspect-ratio Silicon Pillars, Ridges, and Trenches Fabrication suing Ultrahigh E-Beam Lithography and Reactive Ion Etching" *Appl. Phys. Lett.*, **62**(12), 1414, 1993.

[3] P. B. Fischer and S. Y. Chou, "10 nm Electron Beam Lithography and sub-50 nm overlay using a modified scanning election microscope," *Appl. Phys. Lett.*, **62**(23), 2989, 1993.

[4] S. Alexandrou, C. C. Wang, T. Y. Hsiang, M. Y. Liu, and S. Y. Chou, "A 75-GHz Silicon Metal-Semiconductor-Metal Schottky Photodetectors," *Appl. Phys. Lett.*, **62**(20), 2507, 1993.

[5] S. Y. Chou and Y. Wang, "A Planar Double Gate Quantum Wire Transistor," *Appl. Phys. Lett.*, **63**(6), 788, 1993.

[6] Y. Wang, S. Y. Chou and M. R. Melloch, "Effects of Bias, Temperature, and Construction Potential Shape on 1D Ballistic Transport in a Planar Double-Gate Quantum Wire Transistor," *Superlattices and Microstructures*, 14(2/3), 227-230, 1993.

[7] Y. Wang and S. Y. Chou, "Planar Field Induced Quantum Dot Transistor," *Appl. Phys. Lett.*, **63**(16), 2257, 1993.

[8] P. B. Fischer, and S. Y. Chou, "10 nm Si Pillars Fabricated using E-Beam Lithography, Reactive Ion Etching, and HF Etching," *J. Vac. Sci. and Tech.*,B11(6), 2524, 1993.

[9] Y. Wang, and S. Y. Chou, "Observation of Biased-induced Resonant Tunneling Peak Splitting in a Quantum Dot," *Appl. Phys. Lett.*, **64**(3), 309, 1994.

[10] M. Y. Liu and S. Y. Chou, "140 GHz MSM Photodetectors on SOI with Scaled Active Layer Thickness," *Appl. Phys. Lett.*, **65**(7), 887, 1994.

[11] Y. Wang and S. Y. Chou, "Quantum Wave Band Stop Filter,"*Appl. Phys. Lett.*, **65**(16), 2072-2074, 1994.

[12] Y. Wang, W. Y. Deng, and S. Y. Chou, "Electron Transport Through a Quantum Cavity,"*Superlattices and Microstructures*, **17**(2), 193-196, 1995.

[13] E. Leobandung, L. Gou, Y. Wang, and S. Y. Chou, "Observation of Quantum Effects and Coulomb Blockade in Silicon Quantum-Dot Transistors at Temperatures Over 100 K," *Appl. Phys. Lett.*, **67**(16), 2338-2340, 1995.

[14] E. Leobandung, L. Guo, and S. Y. Chou, "Single Hole Quantum Dot Transisteors in Silicon," *Appl. Phys. Lett.*, **67**(16), 2338-2340, 1995.

[15] E. Leobandung, L. Guo, and S. Y. Chou, "Single Electron and Hole Quantum Dot Transistors Operating above 110K," *J. Vac. Sci. and Tech.*, **B13**(6), 2865-2868, 1995.

Conference Papers

[1] S. Y. Chou and Y.Wang. "A New Single Electron Transistor," The 50 th Device Research Conference, Cambridge, Mass, June 22-24, 1992

[2] P. B. Fischer and S. Y. Chou, "Sub-50 nm High Aspect-ratio Silicon Pillars, Ridges, and Trenches Fabrication suing Ultrahigh E-Beam Lithography and RIE," 1992 Int'l Conf. on solid State Devices and Materials, Tsukuba, Japan, August 26-28, 1992.

[3] S. Y. Chou and Y. Wang. "A New Single Electron Transistor," 1992 Int'l Conf. on solid State Devices and Materials, Tsukuba, Japan, August 26-28, 1992.

[4] S. Y. Chou, Y. Liu, W. Khalil, P. B. Fischer, T. Y. Hsiang, S. Alexander, and R. Sobolewski. "Nanoscale Sub-Picosecond Metal-Semiconductor-Metal Photodetectors," 1992 Int'l Conf. on solid State Devices and Materials, Tsukuba, Japan, August 26-28, 1992.

[5] P. B. Fischer and S. Y. Chou, "10 nm Electron Beam Lithography," Int. Conf. on Microcircuit Entering, Erlangen, Germany, Sept. 21-24, 1992

[6] P. B. Fischer and S. Y. Chou, "Sub- 40 nm RIE," Int. Conf. on Microcircuit Entering, Erlangen, Germany, Sept. 21-24, 1992

[7] M. Y. Liu, S. Y. Chou, S. Alexander, and T. Y. Hsiang, "Nanoscale Metal-Semiconductor-Metal Photodetectors with Nanometer Scale Finger Spacing and Width," *Picosecond Electronics and Optoelectronics Topical Meeting*, San Francisco, January 25-27, 1993, *OSA Proceedings on Ultrafast Electronics & Optoelectronics,* Vol. 14, pp. 53-55, 1993.

[8] P. B. Fischer, and S. Y. Chou, "10 nm Si Pillars Fabricated using E-Beam Lithography, Reactive Ion Etching, and HF Etching," The 37th Int'l Symp. on Electron, Ion and Photo Beams, San Diego, CA, June 1-4, 1993.

[9] Y. Wang, and S. Y. Chou, "A New Quantum-Dot Transistor" The 51st Device Research Conference, Santa Barbara, June 21-23, 1993

[10] M. Y. Liu, S. Y. Chou, S. Alexander, C.C. Wang, and T.Y. Hsiang, "110 GHz Si MSM Photodetectors" The 51st Device Research Conference, Santa Barbara, June 21-23, 1993

[11] S. Y. Chou, "Nanostructure Engineering and Applications," Invited talk, 1993 Int'l Microprocess Conf. Hiroshima, Japan, July 19-22, 1993.

[12] E. Leobandung, L. Guo, Y. Wang, and S. Y. Chou, "77 K Silicon Quantum-Dot Transistors," 39th E, EIPB, Scottsdale, AZ, May 31-June 2, 1995.

[13] E. Leobandung, L. Guo, Y. Wang, and S. Y. Chou, "Silicon Quantum-Dot Transistors operating Above 100 K," DRC, Charlottsvile, VA, June 1995.

IV. List of Participating Scientific Report

Principal Investigator: Professor Stephen Chou

Graduate Student: Yun Wang and Effendi Leobandung

V. Advanced Degrees Awarded to Personnel on the Project

M.S. Degree:

Yun Wang

Effendi Leobandung

Ph. D. Degree:

Yun Wang

VI. Invention Disclosure

None